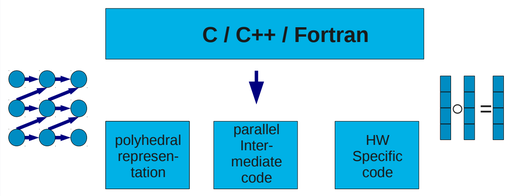
enHance

enabling heterogeneous hardware acceleration using novel programming and scheduling models

using LLVM COMPILER INFRASTRUCTURE

PROJECT TOPICS & WORKING PACKAGES

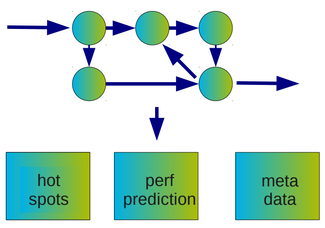
Automatic Program Analysis and Semi-Automatic Parallelization

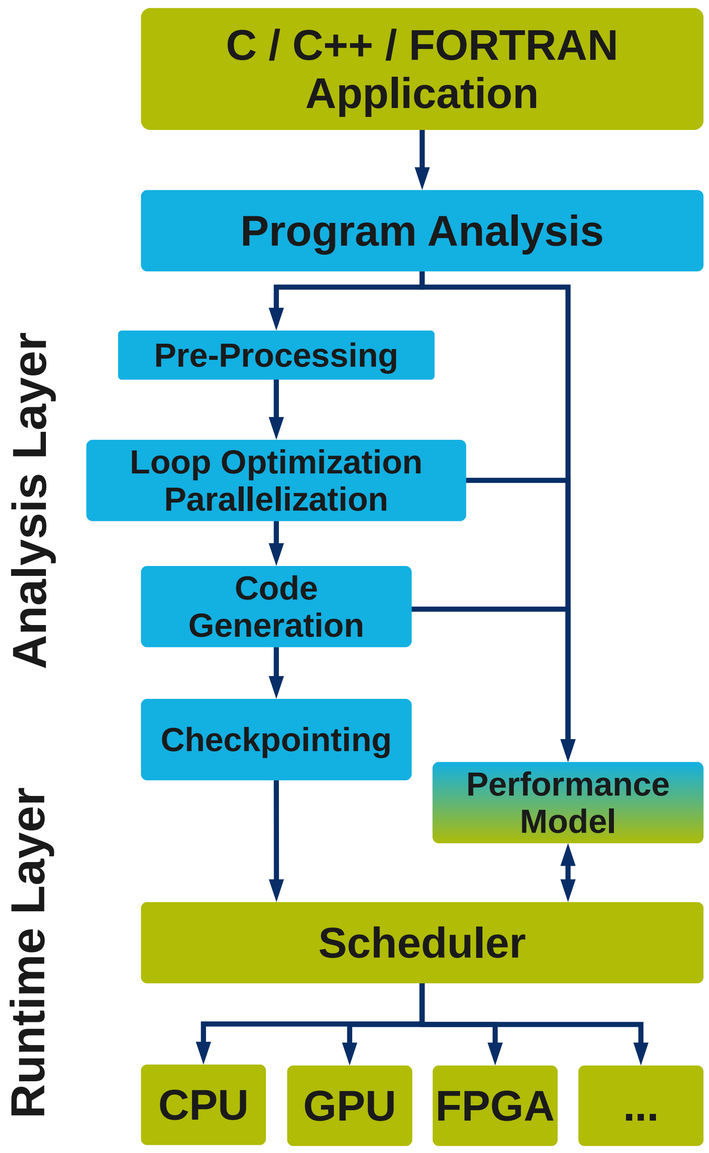


Parallelization for SIMD and Multi-Core as well as cache optimization through PluTo-Library support with PluTo-SICA extension and other polyhedral optimizers in LLVM

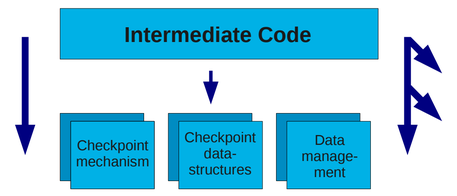
Performance modeling implements determination of run-times by static analysis with LLVM and the automated estimation of object memory footprints alongside with their data-direction

Performance Modeling and Generic Components





Checkpointing Detection and Insertion

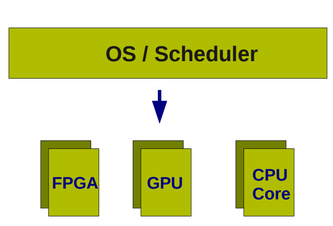


The checkpoint is based on the static analysis inside LLVM

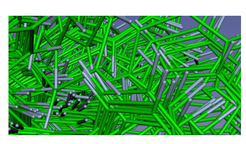
(def-use, use-def)

We instrument the code with the LLVM Functions, BasicBlock, Instruction manipulation to insert the user space scheduler calls

Resource Management and Scheduling

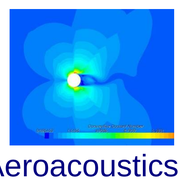


Applications

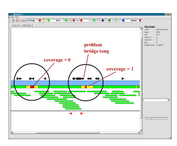


Thermodynamics

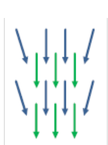
Particle Dynamics



Aeroacoustics



Genome Analysis



Map Reduce Framework

- Project targets a system platform with **Multi-Core, GPU & FPGA** processing devices
- **OS** should **schedule** tasks on different processing devices depending on available resources
- Kernel **metadata** support decision making
- Support the application developer by a **tool-chain** with **semi-automatic parallelization** capabilities
- Optimization of **loops** by **transforming memory access patterns**
- **Hardware aware** transformations and optimization approach

THE ENHANCE CONSORTIUM

TWT GmbH Science & Innovation

GETLIG & TAR

tms technisch-mathematische studiengesellschaft mbh

PC² PADERBORN CENTER FOR PARALLEL COMPUTING

JOHANNES GUTENBERG UNIVERSITÄT MAINZ

Fraunhofer SCAI

ZIB

CeBiTec

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PROJECT DURATION

April 2011 – September 2013

Openfpga member

http://www.enhance-project.de